

Pigeon Point® BMR-P1AFS-ATCA Reference Design Board Management Reference Design for AdvancedTCA®

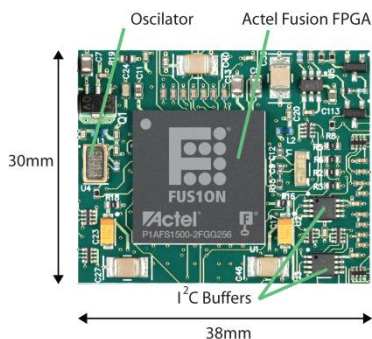
The BMR-P1AFS-ATCA design is one of a series of Pigeon Point Board Management Reference designs. This member of the series provides an IPM Controller (IPMC) for AdvancedTCA and is based on the Fusion mixed-signal FPGA from Microsemi Corporation.

This reference design is delivered in a Pigeon Point Board Management Starter Kit (which is detailed in a separate Product Brief). The kit includes:

- An FPGA design for a Fusion mixed-signal FPGA, implementing the core of an IPM Controller, including a Cortex-M1 ARM processor and supporting peripherals. This design is ready to be adapted for your ATCA board or other intelligent Field Replaceable Unit (FRU).
- Schematics for a corresponding IPM Controller subsystem, ready for integration into the schematic for your board, with adaptation as necessary.
- Firmware for that subsystem, delivered in source form and with development tools—ready for simple and quick adaptation to the specific requirements of your product.
- One-stop support from Pigeon Point Systems for schematics, firmware and software used in developing and delivering your Pigeon Point BMR-based IPM Controller.
- Complementary support from Microsemi for the FPGA design, including adaptations to meet the specific needs of your board.

The photo below shows the core of a BMR-P1AFS-ATCA IPM Controller. The active components are:

- The P1AFS1500 mixed-signal FPGA.
- Dual IPMB buffers to isolate the IPMC from the dual redundant IPMB-0 implemented on the backplane.
- An external oscillator to provide the operating frequency.



Specification compliant and interoperability tested

- PICMG 3.0 R3.0, the AdvancedTCA base specification, plus HPM.1 R1.0, the Firmware Upgrade specification
- IPMI v1.5, document revision 1.1 and the relevant subset of IPMI v2.0, document revision 1.0, plus relevant errata
- Thoroughly tested with other management components at PICMG TCA-IWs (Interoperability Workshops)
- Compliance tested with Polaris Networks' ATCA Tester

Full support for core hardware requirements

- Supports P1AFS600/1500 variants, including FG256 and FG484 packages, with and without external SRAM
- Advanced IPMI over LAN (including Serial over LAN and HPM.1 upgrades) via either non-proprietary Network Controller Sideband Interface (NC-SI) or Intel-proprietary SMBus sideband interface to payload NCs
- Payload voltage monitoring (including 48V supply)
- Thermal sensors (internal Fusion temperature monitors with external bipolar transistors and/or external DS75 digital sensors)
- Analog offload subsystem that does PICMG- and IPMI-aware monitoring of designated Fusion analog sensors without using Cortex-M1 processor cycles
- ATCA hot swap interfaces (handle and blue LED)
- Dual redundant IPMB-0
- Hardware address detection from backplane
- FRU LED management
- Payload power supply controls (multiple voltage levels)
- Control of E-Keying governed fabric interfaces
- Optional persistence of above controls across IPM Controller resets, optionally using SEEPRM storage
- Optional local System Event Log (SEL)
- Optional infrastructure for non-intelligent Rear Transition Modules
- UART- or LPC/KCS-based payload interface
- UART-based serial debug interface

Optional support for special purpose functionality

- Telco (dry contact) alarm management, including choice of IPMI interfaces: PICMG 3.0 R3.0 defined or Pigeon Point proprietary
- Shelf FRU information SEEPRM access

Small footprint and low power

- Core IPMC can fit in 30mm x 38mm footprint
- Maximum current consumption for active components is about 161mA, assuming a P1AFS600 operating with the supplied FPGA design and using the default 25 MHz input clock

Analog offload subsystem eliminates Cortex-M1 processor cycles for monitoring analog sensors

- Separate CoreABC controller monitors up to 30 Fusion analog inputs and checks readings against IPMI-defined thresholds
- Only readings that cross thresholds result in interrupts to the Cortex-M1 processor, potentially eliminating substantial processor load
- Fully configurable sensor sampling and threshold details

Instance-specific information storage in Fusion FlashROM

- Optional support in firmware for retrieving instance-specific information (such as a board serial number) from special 1 Kbit FlashROM area that can only be written via JTAG
- Coordinates with Microsemi tool facilities to allow automatic serializing of successively programmed Fusion devices

Adaptable and extendable FPGA design

- Initial FPGA design provided in several variants (e.g. for different package sizes), can be used directly or modified
- Potential modifications include adding or removing Microsemi IP blocks, adding custom logic and/or IP blocks, changing device pin assignments, if necessary

Comprehensive, readily adaptable firmware

- All mandatory and many optional IPMI/ATCA commands supported over IPMB-0
- Numerous Pigeon Point extension commands, primarily used over the payload and serial debug interfaces
- Payload alert notifications over payload interface for sensor events and receipt of reset/shutdown commands
- PICMG HPM.1 firmware upgrade support
- Simple—but highly flexible—configuration of firmware features

Sophisticated, HPM.1-compliant support for firmware upgrades

- Firmware upgrades over any IPMI interface to the IPM Controller, with redundant copies and automatic fallback after failed upgrade
- IPM Controller is fully functional during upgrade
- Bootloader can be upgraded without using JTAG
- Framework for managing firmware upgrades that include changes in data structures that are preserved across IPMC resets to eliminate disruptive upgrades
- IPMC FRU Information implemented as additional HPM.1 component, allowing FRU Information upgrades independently of firmware
- Optional upgrades via IPMI over LAN interface
- Open source `ipmitool` supplied as upgrade agent
- HPM.1 compliance means that any compliant upgrade agent can upgrade any compliant IPM Controller

Optional support for non-intelligent Rear Transition Modules (RTM)

- Includes specific hardware and firmware support for interface between front board and RTM
- Assumes no management controller on RTM; RTMs equipped with Module Management Controller need corresponding BMR-H8S-AMC facilities (see separate product brief)
- Allows compliance with PICMG 3.0 requirements regarding how an RTM is represented by the IPMC

Choice of serial interface protocols (SIPL variants) supported via UARTs to payload processor and serial debug interface

- SIPL-TM, based on IPMI-defined Terminal Mode of the Serial/Modem Interface,
- SIPL-BM based on IPMI-defined Basic Mode,
- Either protocol selectable individually for either serial interface
- SIPL-TM: human-oriented and ASCII-based, intended primarily for the serial debug interface
- SIPL-BM: machine-oriented and binary-based, intended primarily for the UART-based payload interface
- Both protocols use encoded forms of raw IPMI messages, which are handled by the IPM Controller essentially like IPMB messages

Optional use of LPC/KCS for payload interface¹

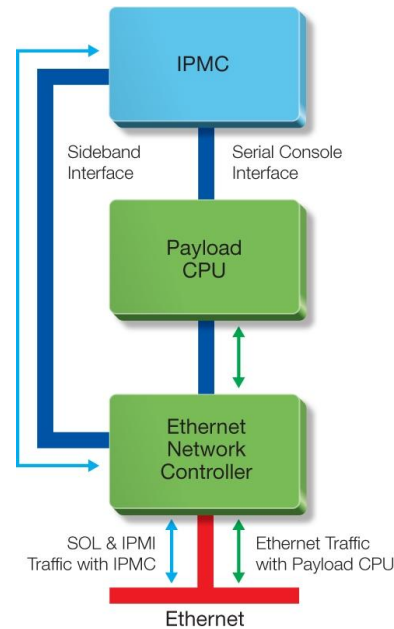
- Enabled in lieu of UART-based payload interface
- Based on IPMI-defined KCS variant of IPMI System Interface, implemented over LPC in Microsemi DirectCore CoreLPC
- Facilitates use of existing IPMI software on payload processor, which often interfaces with management controller via KCS

Optional Simple Network Stack

- Ethernet layer, including drivers for Microsemi Core10/100 Ethernet MAC and for SMBus sideband link to Intel 8257x Network Controllers
- Internet Protocol (IP) layer, which cooperates with ARP module to resolve IP address to MAC addresses
- IP-based protocol layer, including UDP and ICMP
- Provides foundation for application protocols, such as RMCP and RMCP+

Optional IPMI over LAN

- Primary client of simple network stack
- IPMI 2.0 compliant implementation of extended Remote Management Control Protocol (RMCP+), including session establishment
- RMCP+ compliant authentication, integrity and confidentiality, specifically via the following algorithms (all using IPMI 2.0-compliant random number generation):
 - Authentication: HMAC-SHA1
 - Integrity: HMAC-SHA1-96
 - Confidentiality: AES-CBC-128
- IPMI over LAN and SoL payload types in RMCP+, with framework for supporting further payload types
- Enables HPM.1 firmware upgrades via LAN channel
- Optional IP parameter assignment by appropriately enabled Shelf Manager²
- Supported LAN interfaces with Microsemi Core10/100 Ethernet MAC, loaded in P1AFS1500 and configured for RMII, include:
 - NC-SI³, tested with Intel 82575 NC
 - UMP (Universal Management Port, a Broadcom variant of NC-SI), tested with Broadcom BCM5714C
 - Direct Ethernet, where the LAN connection is dedicated to management traffic, not shared with the payload
- Additional supported LAN interface with P1AFS600/1500 and SMBus sideband interface: Intel-proprietary pass-through



Optional Serial over LAN (SoL)

- Uses IPMI over LAN facility to support Serial over LAN via NC-SI, UMP, or Intel-proprietary pass-through on SMBus or a direct Ethernet connection
 - Requires separate physical UART connection between payload and IPMC
- Configuration support for Intel-proprietary super pass-through mode Serial over LAN with Intel 82571 (where, after configuration, 82571 implements SoL internally)
 - Uses virtual COM port inside Intel 82571 NC, accessed via PCIe
- Open source `ipmitool` supplied as SoL client

Optional local System Event Log (SEL)

- Requires SEEPRM storage on board
- IPMI compliant System Event Log for events generated on the FRU(s) represented by the IPMC
- Can provide a useful historical record of events that have been recorded during operation of a board, perhaps for use in board diagnosis at a maintenance depot
- Events are also forwarded to Shelf Manager, as required by PICMG 3.0

Optional support for persistent modifications to Sensor Data Records

- Non-volatile copy of SDR Repository can be configured in on-board SEEPRM
- Sensor threshold and hysteresis values can be configured dynamically via PPS extension commands, and are thereafter persistent across power cycles and resets of the board

Optional support for payload-controlled sensors

- Allows sensors that are implemented by the payload (e.g. an I²C sensor connected to the payload CPU) but exposed by the IPMC as its own
- Covers discrete and threshold sensors

¹ LPC/KCS implements the IPMI-defined Keyboard Controller Style interface using the Low Pin Count version of the Peripheral Component Interconnect (PCI) bus that is used for access to low speed peripherals such as management controllers.

² The Pigeon Point Shelf Manager, starting with release 2.6.4, can be configured to assign IP address parameters to LAN-attached IPMCs via "Set LAN Configuration Parameters" commands.

³ NC-SI is an open specification published by the Distributed Management Task Force (DMTF, www.dmtf.org).

Optional support for persistent configuration parameters

- Parameters preserve values across IPMC power cycles and resets
- Used for most persistent data, such as serial port parameters, LAN and SoL parameters
- Framework for such treatment of other parameters, including those in custom firmware extensions

Simple, but powerful, firmware configuration mechanisms

- Configuration variables in a single `config.h` source file parameterize and determine inclusion/exclusion of subsystems during firmware image build
- Binary configuration files for FRU Information and Sensor Data Records (SDR) merged into firmware image
- FRU Information and SDR files produced from textual representations by special supplied compilers

Comprehensive Cortex-M1 development environment

- Uses cross GNU C compiler and binary utilities for Cortex-M1 processor
- Linux-based development environment included with BMR-P1AFS-ATCA Starter Kit and downloadable from CodeSourcery
- Windows-based development environment (the Microsemi SoftConsole Integrated Development Environment) available for downloading from Microsemi
- JTAG-based firmware download using Microsemi FlashPro3 JTAG programmer (purchased separately)

Numerous extensions beyond required IPMI/ATCA/HPM.1 commands and functionality

- Graceful Reboot and Issue Diagnostic Interrupt options in FRU Control command
- Get/Set FRU LED State commands for blue LED
- Lamp Test function of Set FRU LED State command
- Cold Reset
- Warm Reset
- Get Device GUID
- Master Write-Read
- Get/Set Sensor Hysteresis
- Get/Set Sensor Thresholds
- Get/Set Sensor Event Enable
- Re-arm Sensor Events
- Get Sensor Event Status
- Get/Set Fan Level
- Get/Set Channel Access
- Get Channel Authentication Capabilities
- Get Channel Info
- Set Channel Security Keys
- Get/Set User Access
- Get/Set User Name
- Set User Password
- Get/Set LAN Configuration Parameters
- Get/Set SOL Configuration Parameters
- Activate/Deactivate Payload
- Get/Set User Payload Access

- Get Channel Payload Support
- Get Channel Payload Version
- Abort Firmware Upgrade
- Get Upgrade Status
- Query Self-test Results
- Query Rollback Status
- Initiate Manual Rollback
- Get Telco Alarm Capability
- Get/Set Telco Alarm State
- Get Telco Alarm Location

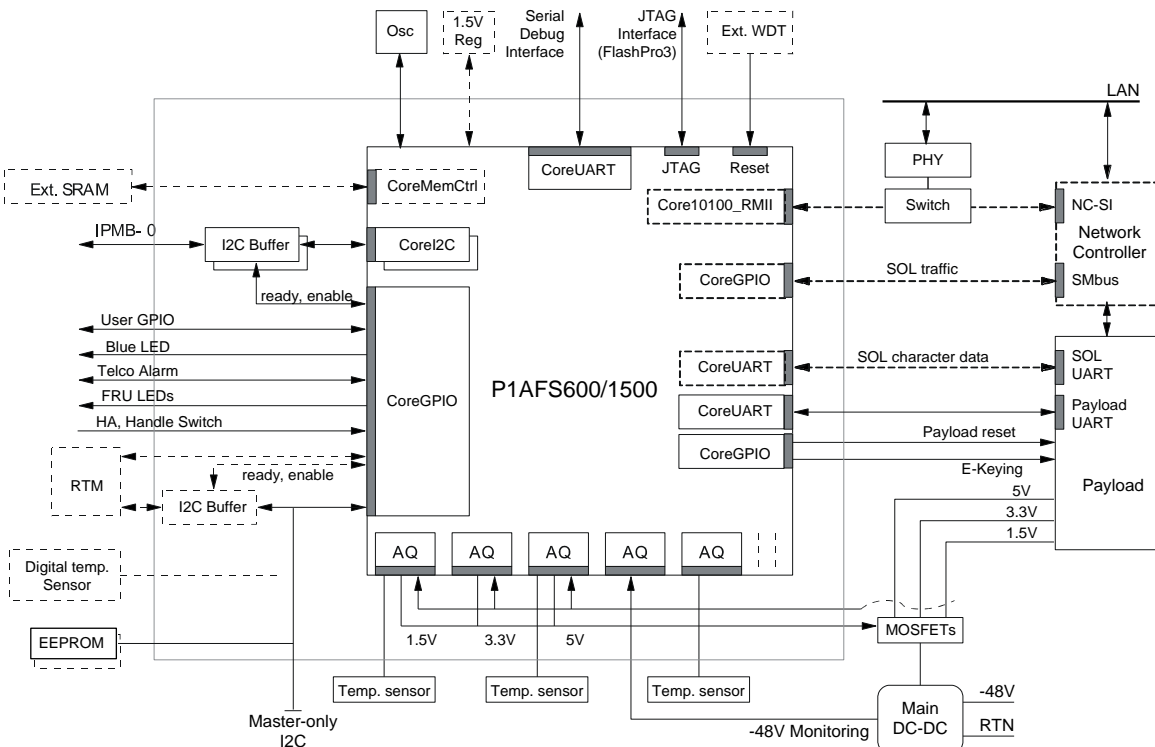
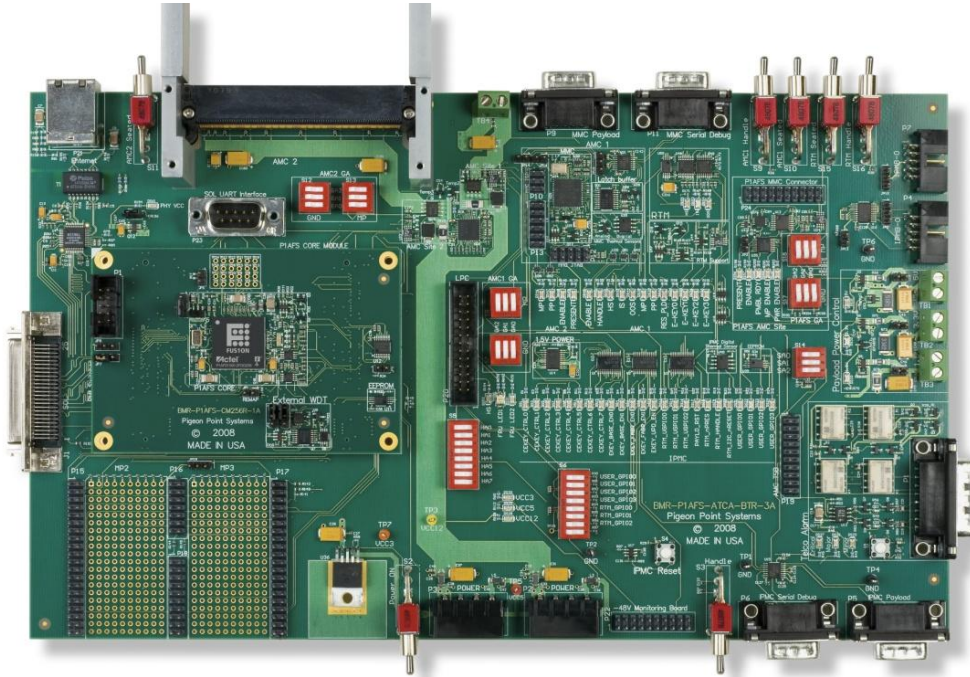
Rich set of Pigeon Point extension commands

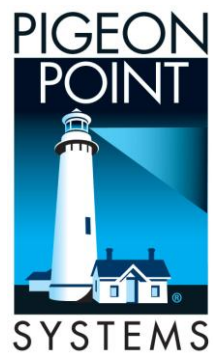
- All extension commands implemented as IPMI-compliant OEM messages
- Get Status
- Get/Set Serial Interface Properties
- Get/Set Debug Level
- Get/Set Hardware Address
- Get/Set Handle Switch
- Get/Set Payload Communication Timeout
- Disable/Enable Payload Control
- Reset IPMC
- Hang IPMC⁴
- Bused Resource Control/Status
- Graceful Reset
- Diagnostic Interrupt Results
- Set/Clear Telco Alarm
- Get Telco Alarm Sensor Number
- Get/Set Payload Shutdown Timeout
- Update Discrete Sensor
- Update Threshold Sensor
- Set EEPROM SDR Data
- Set EEPROM SDR Hysteresis
- Set EEPROM SDR Thresholds
- Reset EEPROM SDR Repository
- Calibrate AFS Temperature Sensor
- Reset Non-Volatile Parameters and Reboot
- Get FPGA Design Version

⁴ This function is used to test the IPMC watchdog.

Reference Implementation

A bench top implementation called the BMR-P1AFS-ATCA-BTR is shown below. In addition to the BMR-P1AFS-ATCA core, the board includes implementations of the optional IPM Controller features and numerous LEDs, switches and headers to allow lab experimentation with the behavior of the IPM Controller. Also on the board are components supporting the BMR-P1AFS-AMC AdvancedMC carrier and BMR-AVR-AMCm AdvancedMC module reference designs. Below the photo is a block diagram of a BMR-P1AFS-ATCA based IPM Controller.





For more information, visit our website at <http://www.pigeonpoint.com>

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