Pigeon Point® BMR-A2F-EMMC-CU Reference Design
Board Management Reference Design for µTCA™ Cooling Units and OEM Modules

The BMR-A2F-EMMC-CU design is one of a series of Pigeon Point Board Management Reference designs. This member of the series provides an Enhanced Module Management Controller (EMMC) for a µTCA Cooling Unit or OEM module and is based on the SmartFusion intelligent mixed signal FPGA from Microsemi Corporation.

This reference design is delivered in a Pigeon Point Board Management Starter Kit (which is detailed in a separate Product Brief). The kit includes:

- A SmartFusion FPGA design that implements the core of an EMMC, working with the Cortex-M3 ARM processor and supporting peripherals in the microcontroller subsystem (MSS). This design is ready to be adapted for your µTCA FRU.
- Schematics for a complete EMMC subsystem, ready for integration into your design, with adaptation as necessary.
- Firmware for that subsystem, delivered in source form and with development tools—ready for simple and quick adaptation to the requirements of your product.
- One-stop support for hardware, firmware and software used in developing and delivering your Pigeon Point BMR-based EMMC.
- Complementary support from Microsemi for the FPGA design, including adaptations to meet the specific needs of your board.

The photo shows the BMR-A2F-EMMC-CU core. The active components are:

- The A2F200 intelligent mixed signal FPGA.
- Dual IPMB buffers to isolate the EMMC from the dual redundant IPMB-0 implemented on the backplane.
- An external oscillator to provide the operating frequency.
Specification compliant and interoperability tested

- PICMG MTCA.0 R1.0
- PICMG MTCA.1 R1.0
- PICMG MTCA.3 R1.0
- IPMI v1.5, document revision 1.1, plus relevant errata
- Successfully tested with other management components at PICMG TCA-IW (Telecom Computing Architecture – Interoperability Workshops)

Full support for core hardware requirements

- 32-bit Cortex-M3 operating at 20 MHz for EMMC firmware execution
- Advanced IPMI over LAN (including Serial over LAN, HPM.1 upgrades and IPMB trace access) via either non-proprietary Network Controller Sideband Interface (NC-SI) or Intel-proprietary SMBus sideband interface to payload NCs; primarily relevant to OEM modules
- xTCA- and IPMI-aware monitoring of designated SmartFusion analog sensors via SmartFusion’s programmable analog subsystem, without using Cortex-M3 processor cycles
- Supports A2F200, with CS288, FG256 and FG484 packages
- µTCA hot swap interfaces (handle and blue LED)
- Hardware address detection from backplane
- Payload power supply controls (multiple voltage levels)
- Optional persistence of above controls across EMMC resets
- Dual redundant IPMB-0
- Choice of UART- or LPC/KCS-based payload interface
- UART-based serial debug interface
- Thermal sensors (A2F-based analog and/or DS75 digital)
- Payload voltage monitoring
- FRU LED management

Optional support for special purpose functionality

- Fan management for Cooling Unit application
- Telco alarm management

Small footprint and low power

- Core EMMC can fit in a 31mm x 25mm footprint with the CS288 package
- Active components consume only 135mA of max power
Programmable analog subsystem eliminates Cortex-M3 processor cycles for monitoring analog sensors
- Within Analog Compute Engine, Sample Sequencing Engine (SEE) monitors up to 24 SmartFusion analog inputs, with Post Processing Engine (PPE) configurable to do IPMI-compatible processing of the readings including threshold detection
- Only readings that cross thresholds result in interrupts to the Cortex-M3 processor
- Fully configurable sensor sampling and threshold details, using Microsemi MSS Configurator tool

Instance-specific information storage in SmartFusion FlashROM
- Optional support in firmware for retrieving instance-specific information (such as a board serial number) from special 1 Kbit FlashROM area that can only be written via JTAG
- Coordinates with Microsemi tool facilities to allow automatic serializing of successively programmed SmartFusion devices

Adaptable and extendable FPGA design
- FPGA design can be used directly or modified
- Potential modifications include adding or removing Microsemi IP blocks, adding custom logic and/or IP blocks, changing device pin assignments, if necessary

Comprehensive, readily adaptable firmware
- All mandatory and many optional IPMI/µTCA commands supported over IPMB-0
  - Numerous Pigeon Point extension commands, primarily used over the payload and serial debug interfaces
  - Payload alert notifications over payload interface for sensor events and receipt of reset/shutdown commands
  - Sophisticated support for firmware upgrades in the field
  - Simple—but highly flexible—configuration of firmware features

Choice of serial interface protocols (SIPL variants) supported via UARTs to payload processor and serial debug interface
- SIPL-TM, based on IPMI-defined Terminal Mode of the Serial/Modem Interface,
- SIPL-BM based on IPMI-defined Basic Mode,
- Either protocol selectable individually for either serial interface
- SIPL-TM: human-oriented and ASCII-based, intended primarily for the serial debug interface
- SIPL-BM: machine-oriented and binary-based, intended primarily for the UART-based payload interface
- Both protocols use encoded forms of raw IPMI messages, which are handled by the EMMC essentially like IPMB messages

Optional use of LPC/KCS¹ for payload interface
- Implemented in lieu of UART-based payload interface
- Based on IPMI-defined KCS variant of IPMI System Interface, implemented over LPC
- Facilitates use of existing IPMI software on payload processor, which often interfaces with management controller via KCS

Sophisticated, HPM.1-compliant support for firmware upgrades
- Firmware upgrades over any IPMI interface to the EMMC, with redundant copies and automatic fallback after failed upgrade
- EMMC is fully functional during upgrade
- Bootloader can be upgraded without using JTAG
- Framework for managing firmware upgrades that include changes in data structures that are preserved across EMMC resets to eliminate disruptive upgrades
- EMMC FRU Information implemented as additional HPM.1 component, allowing FRU Information upgrades independently of firmware
- Optional upgrades via IPMI over LAN interface
- Open source ipmitool supplied as upgrade agent
- HPM.1 compliance means that any compliant upgrade agent can upgrade any compliant EMMC

Optional Simple Network Stack
- Ethernet layer, including drivers for SmartFusion Ethernet MAC and for SMBus sideband link to Intel 8257x Network Controllers
- Internet Protocol (IP) layer, which cooperates with ARP module to resolve IP address to MAC addresses
- IP-based protocol layer, including UDP and ICMP
- Provides foundation for application protocols, such as RMCP and RMCP+

¹ LPC/KCS implements the IPMI-defined Keyboard Controller Style interface using the Low Pin Count version of the Peripheral Component Interconnect (PCI) bus that is included on some processors for access to low speed peripherals such as management controllers.
Optional IPMI over LAN
- Primary client of simple network stack
- IPMI 2.0 compliant implementation of extended Remote Management Control Protocol (RMCP+), including session establishment
- RMCP+ compliant authentication, integrity and confidentiality, specifically via the following algorithms (all using IPMI 2.0-compliant random number generation):
  - Authentication: HMAC-SHA1
  - Integrity: HMAC-SHA1-96
  - Confidentiality: AES-CBC-128
- IPMI over LAN and SoL payload types in RMCP+, with framework for supporting further payload types
- Enables HPM.1 firmware upgrades and IPMB trace access via LAN channel
- Optional IP parameter assignment by appropriately enabled Shelf Manager
- Supported LAN interfaces with SmartFusion Ethernet MAC with RMII, include:
  - NC-SI\(^2\), tested with Intel 82575 NC
  - UMP (Universal Management Port, a Broadcom variant of NC-SI), tested with Broadcom BCM5714C
  - Direct Ethernet, where the LAN connection is dedicated to management traffic, not shared with the payload
- Additional supported LAN interface with SMBus sideband interface: Intel-proprietary pass-through

Optional Serial over LAN (SoL)
- Uses IPMI over LAN facility to support Serial over LAN via NC-SI, UMP, or Intel-proprietary pass-through on SMBus or a direct Ethernet connection
- Payload SoL requires separate physical UART connection between payload and EMMC
- SoL for EMMC serial debug interface available, also
- Configuration support for Intel-proprietary super pass-through mode Serial over LAN with Intel 82571 (where, after configuration, 82571 implements SoL internally)
- Uses virtual COM port inside Intel 82571 NC, accessed via PCIe
- Open source ipmitool supplied as SoL client

Simple, but powerful, firmware configuration mechanisms
- Configuration variables in a single config.h source file parameterize and determine inclusion/exclusion of subsystems during firmware image build
- Binary configuration files for FRU Information and Sensor Data Records (SDR) merged into firmware image
- FRU Information and SDR files produced from textual representations by special supplied compilers

Comprehensive Cortex-M3 development environment
- Uses cross GNU C compiler and binary utilities for Cortex-M3 processor
- Linux-based development environment included with BMR-A2F-EMMC-CU Starter Kit and downloadable from CodeSourcery
- Windows-based development environment (the Microsemi SoftConsole Integrated Development Environment) available for download from Microsemi
- JTAG-based firmware download using Microsemi FlashPro3/4 JTAG programmer (FlashPro4 included with Starter Kit)

Numerous extensions beyond required IPMI/µTCA commands and functionality
- Reset/Get/Set BMC Watchdog Timer
- Graceful Reboot and Issue Diagnostic Interrupt options in FRU Control command
- Get/Set FRU LED State commands for blue LED
- Lamp Test function of Set FRU LED State command
- Cold Reset
- Warm Reset
- Get Device GUID
- Get Message
- Get/Set Sensor Hysteresis
- Get/Set Sensor Thresholds
- Get/Set Sensor Event Enable
- Re-arm Sensor Events
- Get Sensor Event Status
- Get/Set Fan Level
- Get IPMB Link Info
- Get Address Info
- Get Telco Alarm Capability
- Get/Set Telco Alarm State

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\(^2\) The Pigeon Point Shelf Manager, starting with release 2.6.4, can be configured to assign IP address parameters to LAN-attached EMCCs via “Set LAN Configuration Parameters” commands.

\(^3\) NC-SI is an open specification published by the Distributed Management Task Force (DMTF, www.dmtf.org) that uses the Reduced Media Independent Interface (RMII) as the physical transport between the network and management controllers.
Rich set of Pigeon Point extension commands

- All extension commands implemented as IPMI-compliant OEM messages
- Get Status
- Get/Set Serial Interface Properties
- Get/Set Debug Level
- Get/Set Hardware Address
- Get/Set Handle Switch
- Get/Set Payload Communication Timeout
- Disable/Enable Payload Control
- Reset EMMC
- Hang EMMC⁴
- Graceful Reset
- Diagnostic Interrupt Results
- Get/Set Payload Shutdown Timer
- Set Test Flags
- Get/Set Geographic Address

⁴ This function is used to test the EMMC watchdog.
Reference Implementation
A bench top implementation called the BMR-A2F-EMMC-CU-BTR is shown below. In addition to the BMR-A2F-EMMC-CU core, the board includes implementations of the optional EMMC features and numerous LEDs, switches and headers to allow lab experimentation with the behavior of the EMMC.

A high level block diagram of an EMMC based on the BMR-A2F-EMMC-CU reference design is shown below.

BMR-A2F-EMMC-CU Enhanced Module Management Controller Block Diagram