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PRODUCT BRIEF

Pigeon Point BMR-A2F-AMCm Reference Design

Board Management Reference Design for Module Management Controllers

Within AdvancedMC and Custom Derivative Module Architectures

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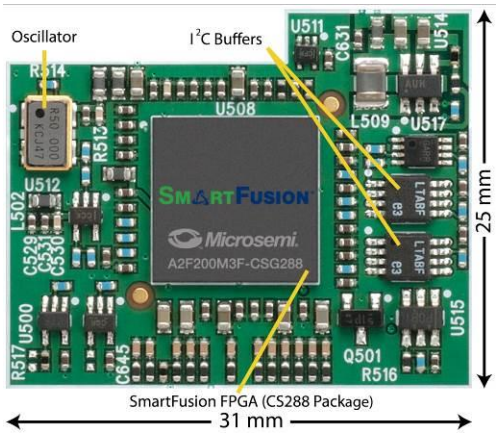
The BMR-A2F-AMCm design is one of a series of Pigeon Point Board Management Reference (BMR) designs. This member of the series provides a Module Management Controller (MMC) for Advanced Mezzanine Cards (AdvancedMCs or AMCs) and custom derivative controllers, based on the SmartFusion intelligent mixed-signal FPGA from Microsemi Corporation.

This reference design is delivered in a Pigeon Point Board Management Starter Kit (which is detailed in a separate Product Brief). The kit includes:

- A SmartFusion FPGA design that implements the core of an MMC, working with the Cortex-M3 ARM processor and supporting peripherals in the microcontroller subsystem (MSS). This design is ready to be adapted for your AMC or custom module.
- Schematics for a complete MMC subsystem, ready for integration into the design of your AMC or custom module, with adaptation as necessary
- Firmware for that subsystem, delivered in source form and with development tools—ready for simple and quick adaptation to the specific requirements of your product
- One-stop support for hardware, firmware and software used in developing and delivering your Pigeon Point BMR-based MMC

The photo below shows the core of an A2F-based IPMC/MMC. The MMC-required active components are:

- An A2F200 intelligent mixed-signal FPGA.
- An external oscillator to provide the operating frequency.
- The I2C buffers are not used in an MMC



Specification compliant and interoperability tested

- AMC.0 R2.0, the AdvancedMC base specification, which covers AdvancedTCA carriers
- MTCA.0 R1.0, the µTCA base specification, which covers µTCA carriers
- PICMG 3.0 R3.0 as amended by ECN 3.0-3.0-001, the AdvancedTCA specification
- HPM.1 R1.0, the PICMG Firmware Upgrade specification
- HPM.2 and HPM.3, the LAN-attached IPM Controller and DHCP-assigned Platform Management Parameters specifications (revisions R1.1 and R2.0, respectively)
- IPMI v1.5, document revision 1.1 and the relevant subset of IPMI v2.0, document revision 1.0, plus relevant errata
- PICMG 3.0, HPM.2/3 and IPMI 2.0 compliance includes support for Internet Protocol version 6 (IPv6)
- Thoroughly tested with other ATCA and µTCA management components at PICMG TCA-IWs (Interoperability Workshops)
- Compliance tested with Polaris Networks' AMC Tester

Highly adaptable, including for custom, derivative management architectures

- Applicable to standard AMCs or custom modules
- Usable with carriers in bladed systems or for carrier-capable main system boards in non-bladed systems, such as appliances
- Independent of number, size and physical form factors of modules
- Module hot swap support available, but need not be used
- Allows integration of standards-based modules with proprietary architecture modules within a single carrier, if desired

Full support for core hardware requirements

- 32-bit Cortex-M3 operating at 40 MHz for MMC firmware execution
- IPMI-aware monitoring of designated SmartFusion analog sensors via SmartFusion's programmable analog subsystem, without using Cortex-M3 processor cycles
- Direct LAN attachment interface or sideband LAN attachment interface implemented via either non-proprietary Network Controller Sideband Interface (NC-SI) or Intel-proprietary SMBus sideband interface to payload NCs, capable of handling IPMI over LAN (including Serial over LAN, HPM.1 upgrades, IPMB trace access and other HPM.2-compliant extensions)
- HPM.2-compliant extended inactive state management, including extended management power support
- Module hot swap interfaces (handle and blue LED)
- Geographic address detection from carrier
- Control of E-Keying governed interfaces (for both fabric and clock E-Keying), with optional persistence across MMC resets
- Managed by on-carrier IPMB-L
- UART- or LPC/KCS-based[1] payload interface
- UART-based serial debug interface
- Thermal sensors (internal SmartFusion temperature monitors with external bipolar transistors and/or external DS75 digital sensors)
- FRU LED management
- EEPROM for persistent data and FRU Information storage (the latter stored in internal ENVM by default)

Small footprint and low power

- Core MMC can fit in the following package-dependent footprints: 25mm x 31mm (CS288), 29.5mm x 34mm (FG256) or 34mm x 44mm (FG484)
- Required active components consume a maximum of 143 mA from management power

Usable on non-module intelligent subsidiary FRUs

- An intelligent subsidiary FRU is represented to an Shelf Manager by an IPMC
- Support for such FRUs consistent with requirements in PICMG 3.0 R3.0
- Example FRU in this category: MMC-equipped Rear Transition Module (RTM)

Programmable analog subsystem eliminates Cortex-M3 processor cycles for monitoring analog sensors

- Within Analog Compute Engine, Sample Sequencing Engine (SEE) monitors up to 32 SmartFusion analog inputs, with Post Processing Engine (PPE) configurable to do IPMI-compatible processing of the readings including threshold detection
- Only readings that cross thresholds result in interrupts to the Cortex-M3 processor
- Fully configurable sensor sampling and threshold details, using Microsemi MSS Configurator tool

Instance-specific information storage in SmartFusion FlashROM

- Optional support in firmware for retrieving instance-specific information (such as a board serial number) from special 1 Kbit FlashROM area that can only be written via JTAG
- Coordinates with Microsemi tool facilities to allow automatic serializing of successively programmed SmartFusion devices

Adaptable and extendable FPGA design

- Initial FPGA design provided in several variants (e.g. for different package sizes), can be used directly or modified
- Potential modifications include adding or removing Microsemi IP blocks, adding custom logic and/or IP blocks, changing device pin assignments, if necessary

[1] LPC/KCS implements the IPMI-defined Keyboard Controller Style interface using the Low Pin Count version of the Peripheral Component Interconnect (PCI) bus that is used for access to low speed peripherals such as management controllers.

Comprehensive, readily adaptable firmware

- All mandatory and many optional IPMI/AMC commands supported over IPMB-L
- Numerous extension commands, primarily used over the payload and debug serial interfaces
- Serial interface protocol based on IPMI Terminal Mode
- Payload alert notifications over payload interface for sensor events and receipt of reset/shutdown commands
- PICMG HPM.1 firmware upgrade support
- Simple—but highly flexible—configuration of firmware features

ASCII-based serial interface protocol supported via UARTs to payload processor and serial debug interface

- Based on IPMI-defined Terminal Mode of the Serial/Modem Interface (and referenced as Serial Interface Protocol Lite—SIPL)
- Same protocol used for both serial interfaces
- Uses ASCII-encoded raw IPMI messages, which are handled by the MMC essentially like IPMB messages

Optional use of LPC/KCS for payload interface

- Enabled in lieu of UART-based payload interface
- Based on IPMI-defined KCS variant of IPMI System Interface, implemented over LPC in Microsemi CoreLPC
- Facilitates use of existing IPMI software on payload processor, which often interfaces with management controller via KCS

Sophisticated, HPM.1-compliant support for firmware upgrades

- Firmware upgrades over any IPMI interface to the MMC, with redundant copies and automatic fallback after failed upgrade
- MMC is fully functional during upgrade
- Bootloader can be upgraded without using JTAG
- Open source ipmitool supplied as upgrade agent
- HPM.1 compliance means that any compliant upgrade agent can upgrade any compliant MMC or other type of IPMC

Optional Simple Network Stack

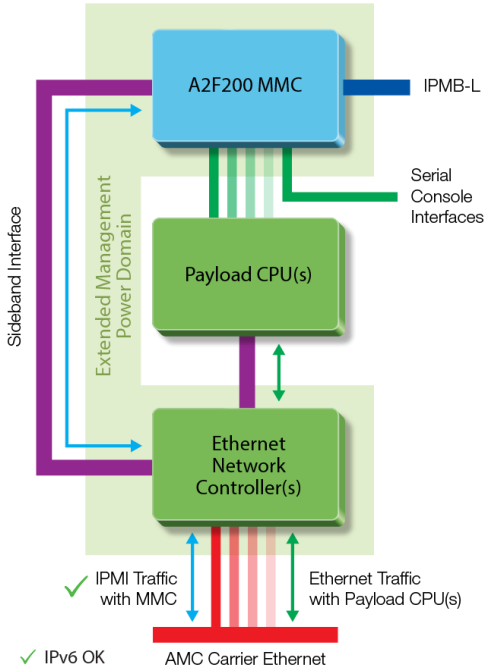
- Ethernet layer, including drivers for SmartFusion Ethernet MAC and for SMBus sideband link to selected Intel NCs
- Internet Protocol (IP) layer, which cooperates with ARP module to resolve IP address to MAC addresses
- IP-based protocol layer, including UDP and ICMP
- Provides foundation for application protocols, such as RMCP and RMCP+

Optional HPM.2 IPMI over LAN

- Primary client of simple network stack
- IPMI 2.0 compliant implementation of extended Remote Management Control Protocol (RMCP+), including session establishment
- RMCP+ compliant authentication, integrity and confidentiality, specifically via the following algorithms (all using IPMI 2.0-compliant random number generation):
  - Authentication: HMAC-SHA1
  - Integrity: HMAC-SHA1-96
  - Confidentiality**:** AES-CBC-128
- IPMI over LAN and SoL payload types in RMCP+, with framework for supporting further payload types
- Enables HPM.1 firmware upgrades and HPM.2 IPMI trace collection via LAN channel
- Optional HPM.3 IPv4 or IPv6 parameter assignment via direct interaction with DHCPv4 or DHCPv6 server or by Shelf Manager[2] or other proxy

[2] The Pigeon Point Shelf can be configured to assign IPv4 address parameters to LAN-attached MMCs via HPM.3-defined mechanisms.

- Supported LAN interfaces with SmartFusion Ethernet MAC with RMII, include:
  - NC-SI[3], tested with selected Intel NCs
  - UMP (Universal Management Port, a Broadcom variant of NC-SI), tested with Broadcom BCM5714C
  - Direct Ethernet, where the LAN connection is dedicated to management traffic, not shared with the payload
  - Additional supported LAN interface with SMBus sideband interface: Intel-proprietary pass-through



Optional support for HPM.2 extended inactive state management and extended management power

- Extended inactive state management support, enables LAN attach facilities (including IPMI over LAN, Serial over LAN and IPMI trace collection) to operate even when MMC-managed FRU is not active (e.g., set up and enabled before payload is powered for first time), greatly increasing diagnostic visibility benefits
- Extended management power support can be implemented in an MMC if LAN attach configuration requires more than specification-defined 150 mA of management power.
  - Carrier IPMC queries each discovered MMC for its extended management power needs
  - If needed, Carrier IPMC enables corresponding Module 12V Payload Power without full payload power authorization, thus leaving the AMC in inactive state
  - Example need scenario: extended management power domain (MMC plus LAN attach Ethernet controller) requires > 150 mA of management power

Optional HPM.2 Serial over LAN (SoL)

- Uses IPMI over LAN facility to support Serial over LAN via NC-SI, UMP, or Intel-proprietary pass-through on SMBus or a direct Ethernet connection
  - Payload SoL requires separate physical UART connection between payload and IPMC
  - SoL for IPMC serial debug interface available, also
  - HPM.2 SOL extensions allow up to 15 concurrent SOL sessions, each with specific serial ports accessible to the MMC, user chosen from up to 255 physical on-board serial ports
- Supplied open source ipmitool can be used as SoL client

Optional local System Event Log (SEL)

- Requires SEEPROM storage on board
- IPMI compliant System Event Log for events generated on the FRU(s) represented by the IPMC
- Can provide a useful historical record of events that have been recorded during operation of a board, perhaps for use in board diagnosis at a maintenance depot
- Events are also forwarded to Shelf Manager, as required by xTCA specifications

[3] NC-SI is an open specification published by the Distributed Management Task Force (DMTF, www.dmtf.org) that uses the Reduced Media Independent Interface (RMII) as the physical transport between the network and management controllers.

Optional support for persistent modifications to Sensor Data Records

- Non-volatile copy of SDR Repository can be configured in on-board SEEPROM
- Sensor threshold and hysteresis values can be configured dynamically via PPS extension commands, and are thereafter persistent across power cycles and resets of the board

Simple, but powerful, firmware configuration mechanisms

- Configuration variables in a single config.h source file parameterize and determine inclusion/exclusion of subsystems during firmware image build
- Configuration data for programmable analog created in MSS Configurator, imported into BMR build
- Binary configuration files for FRU Information and Sensor Data Records (SDR) merged into firmware image
- FRU Information and SDR files produced from textual representations by special supplied compilers

Comprehensive Cortex-M3 development environment

- x86-based Linux-based development environment included with BMR-A2F-AMCm Starter Kit (based on Mentor Graphics Sourcery Code Bench G++ Lite toolchain)
- Windows-based development environment (the Microsemi SoftConsole Integrated Development Environment) available for download from Microsemi
- JTAG-based firmware download using Microsemi FlashPro3/4 JTAG programmer (FlashPro4 included with Starter Kit)

Rich set of Pigeon Point extension commands

- Get Status
- Get/Set Serial Interface Properties
- Get/Set Debug Level
- Get/Set Handle Switch
- Get/Set Payload Communication Timeout
- Disable/Enable Payload Control
- Reset MMC
- Hang MMC
- Graceful Reset
- Diagnostic Interrupt Results
- Get/Set Payload Shutdown Timer
- Get/Set Geographic Address
- Get/Set Payload Shutdown Timeout
- Set Test Flags
- Set EEPROM SDR Data
- Set EEPROM SDR Hysteresis
- Set EEPROM SDR Thresholds
- Reset EEPROM SDR Repository
- Backend Power Control
- Calibrate A2F Temperature Sensor
- Reset Non-Volatile Parameters and Reboot
- Get FPGA Design Version
- Get/Set PWM DAC Level
- Get/Set FRU Info Write-Protect State

Key extensions beyond required IPMI/ATCA/AMC/HPM.1/HPM.2/HPM.3 commands and functionality

- Cold Reset
- Warm Reset
- Get Device GUID
- Get System GUID
- Set User Name
- Get Sensor Reading Factors
- Get/Set Sensor Hysteresis
- Get/Set Sensor Thresholds
- Get/Set Sensor Event Enable
- Re-arm Sensor Events
- Get Sensor Event Status
- Get Sensor Type
- Graceful Reboot and Issue Diagnostic Interrupt options in FRU Control command
- Abort Firmware Upgrade
- Query Self-test Results
- Query Rollback Status
- Initiate Manual Rollback
- HPM.2 Long IPMI Messages
- HPM.2 Extended Inactive State Management
- HPM.2 Dynamic Credentials
- HPM.2 Advanced Discovery
- HPM.2 IPM Controller-Managed Failover
- HPM.2 Multiple SOL Payload Instances
- HPM.2 IPMI Channel Packet Trace Collection

Reference Implementation

The bench top implementation of this reference design is implemented in an AMC form factor, which means that it can be inserted in any compliant AMC slot, including on the BMR-A2F-IPMC BTR bench top board. In addition to the core facilities of the reference designs, the board includes example implementations of the optional controller features and numerous LEDs, switches and headers to allow lab experimentation with the behavior of the controllers, including pre-supported options and any desired firmware customizations. Key lab-oriented features are on the front part of the module and extend forward in front of the carrier for continued access when the board is inserted in an AMC slot. The photo below shows the base BMR-A2F-AMCm bench top board. This board is delivered with an A2F core module mezzanine installed in the center that provides the SmartFusion-based MMC core. A block diagram follows the photo.